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4. Title of the invention

   Signal Processing Apparatus and Method

5. Name of your agent *(if you have one)*

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DUPLICATE

SIGNAL PROCESSING APPARATUS AND METHOD

The present invention relates to a signal processing apparatus and to a method of processing.

There are many applications in which it is required to monitor and analyse a plurality of signals simultaneously. For example, in the pharmaceutical industry an array of 100 or more samples is monitored to determine whether photons are emitted from the samples in response to excitation, and the average delay between excitation and photon emission is measured. Known sample monitoring apparatus includes separate processing apparatus for each sample. For example, a separate correlator is provided for each sample to obtain real-time digital correlation of signals. The provision of separate processing apparatus in respect of each sample is both complicated and expensive.

Generally, a detector head comprising 4 or 8 detectors is used to monitor an array of samples. The number of detectors is limited for two reasons. Firstly, each detector requires a separate correlator, and it is complex and expensive to provide an array of detectors each having respective correlators. Secondly, it is difficult to connect a large number of correlators to a computer. This is because standard computers are generally able to accommodate only 4 correlators, being constrained by the amount of input output space available and by interrupt requirements. Where a detector head comprising 4 or 8 detectors is used, an array of 100 or more samples must be monitored in groups of 4 or 8 samples, and the time required in order to monitor the entire array of samples is significant.

It is an object of the present invention to provide a signal processing apparatus and a signal processing method which overcome the above disadvantage.

According to a first aspect of the invention, there is provided a signal processing apparatus comprising a plurality of input channels each of which is connected to a respective input of a multiplexer, the multiplexer being arranged to

connect each input to a common multiplexer output in a predetermined repeating sequence, and an output circuit connected to the common multiplexer output, wherein the output circuit is arranged to detect the presence at the common multiplexer output of a predetermined signal, to identify the input channel which was the source of the detected predetermined signal, and to output a signal representative of the identified input channel.

The invention allows a large number of signals to be monitored in parallel using relatively simple electronics. By avoiding the need for many parallel correlators, and other parallel electronics, the cost and complexity of monitoring many signals in parallel may be significantly reduced.

The term 'signal processing apparatus' is not intended to mean that the apparatus provides an analysis of data, but rather is intended to include re-ordering of data.

Preferably, a predetermined signal is provided continuously to one input channel of the predetermined sequence, such that the output circuit will output a signal representative of that input channel, referred to hereafter as the marker channel, each time that it is connected to the multiplexer. In this manner, a 'time stamp' is recorded for each cycle of the predetermined sequence. The marker channel is preferably the final input channel of the sequence.

Preferably, each input channel is connected to the multiplexer for a time sufficient to determine whether the predetermined signal is present at the input, but is not connected for a time sufficient to allow a signal representative of that input channel to be output unless the predetermined signal is detected. For example, 2ns may be required to determine whether the predetermined signal is present at the input, and a further 5ns may be required to allow the signal representative of that input channel to be output.

Preferably, if the predetermined signal is detected, the input channel is connected to the multiplexer input for a time sufficient to transfer the signal representative of that input channel to a data latch.

Preferably, the data latch is connected to a storage means.

Preferably, the storage means comprises a plurality of memories, and the signal representative of the identified input channel is allocated to one of the memories via a second multiplexer.

Preferably, the multiplexer is controlled by a counter, and the signal representative of the identified input channel comprises the number generated by the counter.

Preferably, the counter is driven by a clock.

Preferably, the counter is a self-rollover counter arranged to recommence the sequence after a final input channel of the predetermined sequence has been connected to the common multiplexer output.

Preferably, the counter is controlled by an AND gate, a first input of which is connected to the clock, and a second input of which is connected via a NOT gate to the common multiplexer output, so that the counter is incremented by the clock in the absence of the predetermined signal at the common multiplexer output and incrementation of the clock is suspended when the predetermined signal is at the common multiplexer output.

Preferably, at least some of the input channels are connected to detectors.

Preferably, at least one detector includes means to accumulate a signal representative of events incident at that detector.

Preferably, at least one detector is provided with detector reset means arranged to reset that detector once the signal representative of the input channel has been transferred to a data latch.

Preferably, the detector reset means is controlled via a third multiplexer having connections to each of the detectors.

The detectors may be photon multipliers, avalanche photodiodes, hybrid dynode amplified avalanche photodiodes or PIN detectors.

The detectors may be arranged to detect individual quanta, for example photons. The photons may be scattered by a sample being monitored, in which case the scattering of the photons may provide information regarding motion within the sample. Alternatively, the photons may be emitted from a sample as a result of excitation of that sample. Where this is the case, the characteristic lifetime of the photon emission may be measured.

Preferably, the apparatus further comprises data conversion means for converting signals stored in the storage means into a series of sets of data, each set of data being representative of the incidence of the predetermined signal at a particular input channel.

Preferably, the data conversion means comprises a pair of masks and a counter hereafter referred to as the mask counter, a first mask being configured to increment the mask counter when a signal representative of the marker channel of the sequence is output from the memory, and a second mask being configured to transfer the contents of the mask counter to a memory when a signal representative of a predetermined input is output from the memory.

The data conversion means may comprise three masks and a counter hereafter referred to as a mask counter, a first mask being configured to increment the mask counter by a first predetermined amount when a signal representative of the marker

channel of the sequence is output from the memory, a second mask being configured to increment the mask counter by a second predetermined amount when a signal representative of an input channel other than a predetermined input or the marker channel is output from the memory, and a third mask being configured to transfer the contents of the mask counter to a memory when a signal representative of the predetermined input is output from the memory.

Preferably, the mask counter is reset once its contents have transferred to the memory.

According to a second aspect of the invention, there is provided a method of signal processing comprising connecting each of a plurality of input channels in a predetermined repeating sequence to a common multiplexer output via respective multiplexer inputs, and connecting the common multiplexer output to an output circuit, wherein the method further comprises detecting the presence at the common multiplexer output of a predetermined signal, identifying the input channel which was the source of the detected predetermined signal, and outputting a signal representative of the identified input channel.

The method may incorporate any of the above mentioned apparatus.

The invention may be particularly suited to mass assays as used in microbiology, DNA, RNA, novel drug, and novel chemical screening.

A specific embodiment of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic illustration of a processing apparatus according to the invention;

Figure 2 is a schematic illustration of a detector forming part of the processing apparatus shown in Figure 1;

Figures 3a and 3b are schematic illustrations of memory store interrogation circuits which may be used to derive data recorded by the processing apparatus shown in Figure 1; and

Figure 4 is a schematic illustration of an agile frequency transmission system with which the invention may be incorporated.

Figure 1 shows schematically a processing apparatus according to the invention. The processing apparatus includes 128 optical detectors 1 each connected to an input of a multiplexer 2, although only three of the optical detectors 1a-c are shown in Figure 1 for ease of illustration. A final input (input number 128) of the multiplexer 2 is connected to a voltage source 3 which is maintained at a sufficiently high level that the input represents a logical high. The multiplexer 2 has a single output 4, which is connected to a latch 5. The multiplexer 2 is driven by a self-rollover counter 6 (the counter 6 is connected to the multiplexer 2 by a bus). The counter 6 is controlled by an AND gate 8 which is connected to a clock 7 and to a NOT gate 9 arranged to invert the output of the latch 5.

In use, the counter 6 is started and generates an output '1' causing the multiplexer to connect the first optical detector 1a to the output 4. If there is no signal from the first optical detector 1a, the output 4 from the multiplexer 2 remains low. The counter 6 continues to operate and generates an output '2', thereby causing the multiplexer 2 to connect the second optical detector 1b to the output 4. If there is no signal from the second optical detector 1b, the output 4 from the multiplexer 2 remains low. The counter 6 will then cause the multiplexer to connect to the output from the third optical detector 1c to the output 4. This progression will continue for the entire sequence of 128 optical detectors 1 connected to the multiplexer, assuming that there is no signal from the optical detectors 1. When the counter 6 generates an output which corresponds to the number of the final input of the multiplexer 2 (i.e. 128) the voltage source 3 will be connected to the output 4.

When the voltage source 3 is connected to the output 4, the output of the latch 5 goes high, and the output of the NOT gate 9 goes low. The low output from the NOT gate 8 stops operation of the counter 6 via the AND gate 8.

A data latch 10 is connected to the counter 6 and controlled by the latch 5. The data latch 10 is switched on when the output of the latch 5 goes high, and the number generated by the counter 6 is transferred to the data latch 10 via a bus. In the present case, the number transferred to the data latch 10 is '128', i.e. the number of the multiplexer input which is connected to the voltage source 3. The number held in the data latch 10 is transferred to a memory 12. In this example, the memory 12 comprises three separate memories 12a-c, and data is allocated to the separate memories via a second multiplexer 11. The second multiplexer 11 is of the 1 to N type, and is controlled by a multiplexer controller 11a.

The latch 5 may be reset to a low output once the number generated by the counter 6 has been transferred to the data latch 10. The output of the NOT gate 9 will go high when the latch 5 is reset, causing the output of the AND gate 8 to go high, thereby recommencing operation of the counter 6. The counter 6 is of the self-rollover type, and since it has already generated the output '128', it will automatically rollover, and will generate an output '1', followed by '2', etc.. The multiplexer 2 is thus connected again to the outputs of each of the optical detectors 1, as described above. A delay (not shown) may be used to ensure that data has been transferred to the data latch 10 prior to the renewed operation of the counter 6 and multiplexer 2.

If, for example, the output of all of the optical detectors 1 remains low for five cycles of the multiplexer 2, the memory 12 will contain the number '128' five times in succession. The final input channel of the multiplexer 2 is effectively a marker channel which provides an output for each cycle of the multiplexer. If an event is detected at one of the optical detectors 1, then the number generated by the counter 6 representative of that detector 1 will be transferred from the counter 6 via the data latch 10 and the second multiplexer 11 into the memory 12. Thus, for sparse data,

where the likelihood of an optical detector 1 detecting a photon is low, the contents of the memory 12 may, for example, be as follows:

128, 128, 128, 36, 128, 93, 128, 128, 128, 7, 128.........

To maximise the temporal resolution of the circuit, the frequency of the counter 6 is set as high as possible. The limiting factor for the counter frequency is the speed of operation of the latch 5. The counter frequency must be such that when the multiplexer 2 provides a high output, the counter 6 is stopped before it increments further, so that the number at the counter 6 may be transferred to the data latch 10.

Data is allocated to the memory 12 by the second multiplexer 11, which is controlled by the multiplexer controller 11a. The multiplexer may operate in two different modes.

In a first mode of operation, the first memory 12a is provided with data until full, whereupon the data is directed to the second memory 12b, after which data is sent to the third memory 12c. Further memories (not shown) may be used as required. The plurality of memories 12a-c is advantageous because data may be transferred from one memory, for example memory 12a, and analysed whilst another memory, for example memory 12b, is being filled, so that analysis of data in the memories 12a-c is seamless.

In a second mode of operation, a first data element is directed by the multiplexer 11 to the first memory 12a, and a subsequent data element is directed by the multiplexer 11 to the second memory 12b. A third data element is directed by the multiplexer 11 to the first memory, 12a, etc., such that data elements alternate between the first and second memories 12a, 12b. This mode of operation is advantageous because it allows data to be transferred to the memory 12 quickly, and is useful when the rate of data arriving at the data latch 10 is greater than the maximum input rate of a single memory. The number of memories may be selected to provide a required maximum memory input rate.

A third multiplexer (not shown) is arranged to operate in parallel with the first multiplexer 2 and is of the 1 to N type. The third multiplexer is incremented by the counter 6. Each output of the third multiplexer is connected to a reset input of an optical detector 1, in a configuration corresponding to the connection of the optical detectors 1 to the first multiplexer 2. The input of the third multiplexer is connected to the latch 5 such that an optical detector 1, having detected an event, is reset once the counter output number specifying that detector 1 has been transferred to the data latch 10.

The optical detectors 1 shown in Figure 1 are required to provide a latched high output when an optical event is detected. A suitable circuit for an optical detector 1 is shown in Figure 2. A photon counting detector 13 is connected via an amplifier 14 to a switch 15. When the switch 15 is in the configuration shown in Figure 2 the output from the amplifier 14 is connected to a discriminator 16 followed by a pre-scaling circuit 17. The output from the pre-scaling circuit 17 is connected via an OR gate 18 to a latch 19 . In the first configuration, the circuit provides a latched high output when a predetermined number of photons have been detected. When the switch is in the opposite configuration to that shown, the output from the amplifier 14 is connected to one side of a capacitor 20. An opposite side of the capacitor 20 is connected via a discriminator 21 to the OR gate 18 and from there to the latch 19. In the second configuration, the circuit provides a latched high output when a certain analogue integral of photons has been detected.

The circuit shown in Figure 2 is provided merely as an example, and other circuits may be arranged to provide a latched high output in response to detected events. Such circuits may include digital pre-scaling integration and differentiation, linear or non-linear operation of the amplifier, and signal multiplication or inversion.

A circuit suitable for analysing the contents of the memory 12 is shown in Figure 3a. The circuit comprises two digital masks 22, 23, a counter 24 connected to the output of the digital masks 22, 23 and an output buffer 25. In use, the first digital

mask 22 is configured to provide a high output only when a number representative of the marker channel input of the first multiplexer 2 (i.e. input 128) is read. The output from the first mask 22 causes the counter 24 to increment each time the number '128' is output from the memory 12. The second digital mask 23 is configured to provide a high output whenever the memory 12 outputs a number corresponding to a pre-selected detector (for example detector number 73). When the memory outputs the number corresponding to the pre-selected detector, the second mask 23 provides a high output. The high output from the second mask 23 causes the content of the output buffer 25 to be read, and the counter 24 to be reset. Thus the output buffer 25 outputs a number which corresponds to the number of cycles of the multiplexer 2 which occur between the detection of events at the pre-selected detector.

The rate at which data may be output from the memory 12 is limited by the speed of operation of the counter 24. The output of the second mask 23 may be connected to a delay circuit (not shown) arranged to stop data being output from the memory 12 until the contents of the output buffer have been read and the counter 24 has been reset.

Once the memory 12 has been interrogated in relation to a pre-selected detector (for example, detector number 73 as described above), the second digital mask 23 is set to interrogate the memory 12 for a further pre-selected detector, for example number 74. A plurality of mask pairs (not shown in Figure 3a) may be used to analyse simultaneously the memory store 12 in relation to a plurality of pre-selected detectors.

A described in relation to Figure 1, the memory 12 may comprise a set of memories 12a-c. Where this is the case, the memory 12 may be arranged that a first memory 12a is interrogated whilst a second memory 12b is being filled with data. If the interrogation is sufficiently fast, it will be completed before the second memory 12b is filled. The first memory may then be filled with data as the second memory 12b is interrogated, etc.. In this manner it is possible to continuously analyse the array of detectors 1 using a processing apparatus having only two memories 12a, 12b.

Data from the output buffer 25 may be analysed using a pulse arrival distribution or other analysis method, and the results directed to a memory store having addresses corresponding to pre-selected detectors. A non-linear timing circuit, as described in PCT/GB98/03093, may be used to analyse data quickly, and to convert data into a compact form.

The processing apparatus according to the invention may be used for a number of applications. Several of these applications are described below; other applications will be apparent to those skilled in the art.

The processing apparatus may be used to detect photons emitted by an array of 100 biological samples. This may be done for example using the apparatus as illustrated in Figure 1, with 100 detectors 1 connected to the multiplexer 2. In an advantageous arrangement, the clock 7 is set to increment the counter 6 every 2ns (2ns being the time required to determine whether the output of a detector 1 is high) so that the time required to scan the 100 detectors 1 is 200ns. If the output from a detector is high, the time taken to transfer the number at the counter 6 to the memory 12 is 5ns. Thus, it takes approximately 205ns to "scan" the multiplexer 2, assuming that no events are detected (the extra 5ns corresponds to the final input of the multiplexer, which is connected to the voltage source 3).

Assuming an average of 10,000 photon counts per detector per second, the total photon input to the processing apparatus would be 1,000,000 photons per second. Since the number of photons arriving at the detectors is approximately 1,000,000 per second, a photon will on average be detected once every five scans. Thus, the band width of each optical detector is approximately 5 MHz. This bandwidth is ideally suited to photon correlation and number fluctuation spectroscopy measurements.

Seamless and continuous analysis of data from the processing apparatus, if the data is analysed by a single analysis circuit using a single pair of masks as described

above in relation to Figure 3a would require an analysis circuit operating at 100 MHz. Signal processors which operate in this frequency range are known in the art.

The circuit shown in Figure 3a is useful for analysing the contents of the memory 12 when the probability of more than one event being detected during a single scan of the first multiplexer 2 is low. Whenever an event is detected during a cycle of the multiplexer, the time taken for that cycle to be completed will be longer than the time required to complete the cycle if no event were detected. This is because time is required to transfer the number representative of the relevant detector to the data latch 10. This increase of the cycle time has very little effect on the accuracy of the time recorded for a given event when the probability of more than one event being detected during a single scan of the first multiplexer 2 is low. However, where the apparatus is used to detect data which is not sparse, then the accuracy of the time measurement will reduce as the density of that data increases.

Figure 3b shows a circuit which will provide an accurate time measurement irrespective of whether or not the data detected by the processing apparatus is sparse. The circuit comprises three digital masks 26-28. A first of these digital masks is configured to provide an output only when a number representative of the highest input of the first multiplexer 2 (i.e. input 128) is read. The mask 26 outputs the number 128, which is input to a counter 29. Thus, for each cycle of the processing apparatus the counter 29 is incremented by 128. The second digital mask 27 is configured to provide an output when a number representative of any of the inputs of the first multiplexer 2, other than input number 128 or the input of interest, is output from the memory. This mask outputs a number representative of the extra time added to that cycle of the multiplexer 2 due to the detection of an unwanted event. In this case the number is 3. Thus, the total number held at the counter 29 is the sum of the number of cycles of the multiplexer 2 multiplied by 128 plus the number of times an event has been detected at a detector other than the detector of interest multiplied by 3. The total time recorded at the counter thus takes account of every event incident at the multiplexer 2.

The third digital mask 28 is configured to provide a high output when a number representative of the detector of interest is output from the memory 12. When this occurs, the contents of an output buffer 30 connected to the counter 29 are read, and the counter 29 is re-set. The output buffer 30 thus outputs a series of numbers which accurately represent the time between successive events at the detector of interest.

Although the invention has been described in relation to the detection and correlation of experimental data, the invention may used in a wide variety of applications. For example, the invention may be used in the field of communications, and may in particular be used to provide rapid frequency scanning.

It is known in the art that communications may be made more secure by the use of so called agile frequency transmission, wherein the frequency of a transmitted signal jumps according to a pre-set pattern. This is done in order to make it difficult for a third party to detect a significant part of a transmitted message. The invention may be used to monitor a plurality of transmission frequencies simultaneously, using a multiplexed array of detectors (as described in relation to Figure 1), and sorting data using masks (as described in relation to Figures 3a and 3b). Data corresponding to one detection frequency may be analysed independently and in combination with data corresponding to other detection frequencies, to allow monitoring of a transmission even where other signals or noise are present within the bandwidth.

A coding apparatus suitable for providing agile frequency transmission is illustrated in Figure 4. Three signal lines 31 are connected to an N to N multiplexer 32 and thence to transmission lines 33 which may be electronic links, radio links, microwave links or a combination of these. The multiplexer 32 is controlled by a random number generator 34 or other suitable coding unit which must be seeded by a seed input 35 prior to transmission. On transmission of a data bit from the multiplexer 31, an OR gate 36 triggers the random number generator 34 to output a new random number such that the multiplexer 32 connects different signal lines 31 to different transmission lines 33.

A suitable decoding apparatus is also shown in Figure 4. Signals arriving on transmission lines 33 are rearranged by an N to N multiplexer 37. The multiplexer is controlled by the seed line 38 which carries the data required to switch between the transmission lines 33 in order to reconstitute the signal. An OR gate 39 increments the multiplexer 37 via a number generator 40 which is controlled by the seed line 38. Output lines 41 from the multiplexer 37 may be connected to the processing apparatus according to the invention. The invention is advantageous because it allows all of the output lines 41 to be monitored simultaneously.

A signal may be further scrambled by performing a logical operation between the input signal lines 31 prior to their being coded by the multiplexer 32. Known coding methods may be combined with the coding apparatus shown in Figure 4. For example, correlation coding may be employed, wherein each data bit is a function of all previous data bits.

In the event that no data is carried by one of the input signal lines 31, random data or a false signal may be generated as decoy data.

Where the apparatus illustrated in Figure 4 is used to encode data for transmission via telephone lines, a programmable multiplexer is advantageous. The programmable multiplexer should have a sufficient number of channels to allow data from all possible telephone lines to be coded simultaneously, but be capable of being configured to remove a multiplexer input from the coding when a telephone line corresponding to that multiplexer input is not in use.

The apparatus illustrated in Figure 4 may be used to provide signal correction. One or a plurality of signals may be arranged to contain a test signature which is measured at a receiver and used as data to correct incoming signals.

The invention may be applied to the transmission of images. In may instances an image may be composed predominantly of low logical signals. This may be

because the majority of the image is dark, or may be because the transmission has been coded such that only changes of pixel values are transmitted. A processing arrangement according to the invention having a multiplexer with a number of channels equal to the number of pixels comprising an image (plus one extra channel to carry a logic high) may be used to transmit the image in an efficient manner.

The invention may be applied to the decoding of television signals. Where a plurality of television signals are being transmitted simultaneously (i.e. several channels), the invention may be used to direct different signals toward different viewing screens or storage devices. The invention thus allows more than one television channel to be viewed simultaneously on different screens, or to be directed to a storage medium.

The invention may be used in any application where signals from many low bandwidth sources are connected to a single high bandwidth processor or transmission line. One such application is in communications, where many low bandwidth telephone lines are connected to a high bandwidth carrier. For example, many copper telephone wires may be connected to a microwave transmitter or a fibre optic cable.

It is preferable in communications to change the coding of a transmitted signal in response to changes of transmission rates (handshaking code and error correction code may also be changed). The invention allows for the collection, storage and decoding of communications signals continuously and seamlessly, thereby allowing the signals to be re-coded prior to re-transmission by a high bandwidth carrier.

Another application in which signals from many low bandwidth sources are coupled to a single high bandwidth connection is the connection of local Internet connections to a server and then the server to the Internet gateway. A further application is the communication between a supercomputer and the outside world where many "slow" people may be accessing the same system. A further application is the connection of an internal phone network to an external network to transfer information between sites. The outgoing phone calls between two company sites may

be suitably coded compressed onto a single phone line and be uncompressed into the required lines when leaving the system.

CLAIMS

1. A signal processing apparatus comprising a plurality of input channels each of which is connected to a respective input of a multiplexer, the multiplexer being arranged to connect each input to a common multiplexer output in a predetermined repeating sequence, and an output circuit connected to the common multiplexer output, wherein the output circuit is arranged to detect the presence at the common multiplexer output of a predetermined signal, to identify the input channel which was the source of the detected predetermined signal, and to output a signal representative of the identified input channel.

2. A signal processing apparatus according to claim 1, wherein a predetermined signal is provided continuously to one input channel of the predetermined sequence, such that the output circuit will output a signal representative of that input channel, referred to hereafter as the marker channel, each time that it is connected to the multiplexer.

3. A signal processing apparatus according to claim 1 or 2, wherein each input channel is connected to the multiplexer for a time sufficient to determine whether the predetermined signal is present at the input, but is not connected for a time sufficient to allow a signal representative of that input channel to be output unless the predetermined signal is detected.

4. A signal processing apparatus according to claim 3, wherein, if the predetermined signal is detected, the input channel is connected to the multiplexer input for a time sufficient to transfer the signal representative of that input channel to a data latch.

5. A signal processing apparatus according to claim 4, wherein the data latch is connected to a storage means.

6. A signal processing apparatus according to claim 5, wherein the storage means comprises a plurality of memories, and the signal representative of the identified input channel is allocated to one of the memories via a second multiplexer.

7. A signal processing apparatus according to any preceding claim, wherein the multiplexer is controlled by a counter, and the signal representative of the identified input channel comprises the number generated by the counter.

8. A signal processing apparatus according to claim 7, wherein the counter is driven by a clock.

9. A signal processing apparatus according to claim 7 or 8, wherein the counter is a self-rollover counter arranged to recommence the sequence after a final input channel of the predetermined sequence has been connected to the common multiplexer output.

10. A signal processing apparatus according to claim 9, wherein the counter is controlled by an AND gate, a first input of which is connected to the clock, and a second input of which is connected via a NOT gate to the common multiplexer output, so that the counter is incremented by the clock in the absence of the predetermined signal at the common multiplexer output and incrementation of the clock is suspended when the predetermined signal is at the common multiplexer output.

11. A signal processing apparatus according to any preceding claim, wherein at least some of the input channels are connected to detectors.

12. A signal processing apparatus according to claim 11, wherein at least one detector includes means to accumulate a signal representative of events incident at that detector.

13. A signal processing apparatus according to claim 11 or 12, wherein at least one detector is provided with detector reset means arranged to reset that detector once the signal representative of the input channel has been transferred to a data latch.

14. A signal processing apparatus according to claim 13, wherein the detector reset means is controlled via a third multiplexer having connections to each of the detectors.

15. A signal processing apparatus according to claim 5 or any claim dependent thereon, further comprising data conversion means for converting signals stored in the storage means into a series of sets of data, each set of data being representative of the incidence of the predetermined signal at a particular input channel.

16. A signal processing apparatus according to claim 15, wherein the data conversion means comprises a pair of masks and a counter hereafter referred to as the mask counter, a first mask being configured to increment the mask counter when a signal representative of the marker channel of the sequence is output from the memory, and a second mask being configured to transfer the contents of the mask counter to a memory when a signal representative of a predetermined input is output from the memory.

17. A signal processing apparatus according to claim 15, wherein data conversion means comprises three masks and a counter hereafter referred to as a mask counter, a first mask being configured to increment the mask counter by a first predetermined amount when a signal representative of the marker channel of the sequence is output from the memory, a second mask being configured to increment the mask counter by a second predetermined amount when a signal representative of an input channel other than a predetermined input or the marker channel is output from the memory, and a third mask being configured to transfer the contents of the mask counter to a memory when a signal representative of the predetermined input is output from the memory.

18. A signal processing apparatus according to claim 16 or 17, wherein mask counter is reset once its contents have transferred to the memory.

19. A method of signal processing comprising connecting each of a plurality of input channels in a predetermined repeating sequence to a common multiplexer output via respective multiplexer inputs, and connecting the common multiplexer output to an output circuit, wherein the method further comprises detecting the presence at the common multiplexer output of a predetermined signal, identifying the input channel which was the source of the detected predetermined signal, and outputting a signal representative of the identified input channel.

20. A method of signal processing according to claim 19, and incorporating the apparatus as claimed in any of claims 1 to 18 .

21. A signal processing apparatus substantially as hereinbefore described with reference to the accompanying figures.

22. A method of signal processing substantially as hereinbefore described with reference to the accompanying figures.

ABSTRACT

A signal processing apparatus comprising a plurality of input channels each of which is connected to a respective input of a multiplexer, the multiplexer being arranged to connect each input to a common multiplexer output in a predetermined repeating sequence, and an output circuit connected to the common multiplexer output, wherein the output circuit is arranged to detect the presence at the common multiplexer output of a predetermined signal, to identify the input channel which was the source of the detected predetermined signal, and to output a signal representative of the identified input channel.

Figure 1

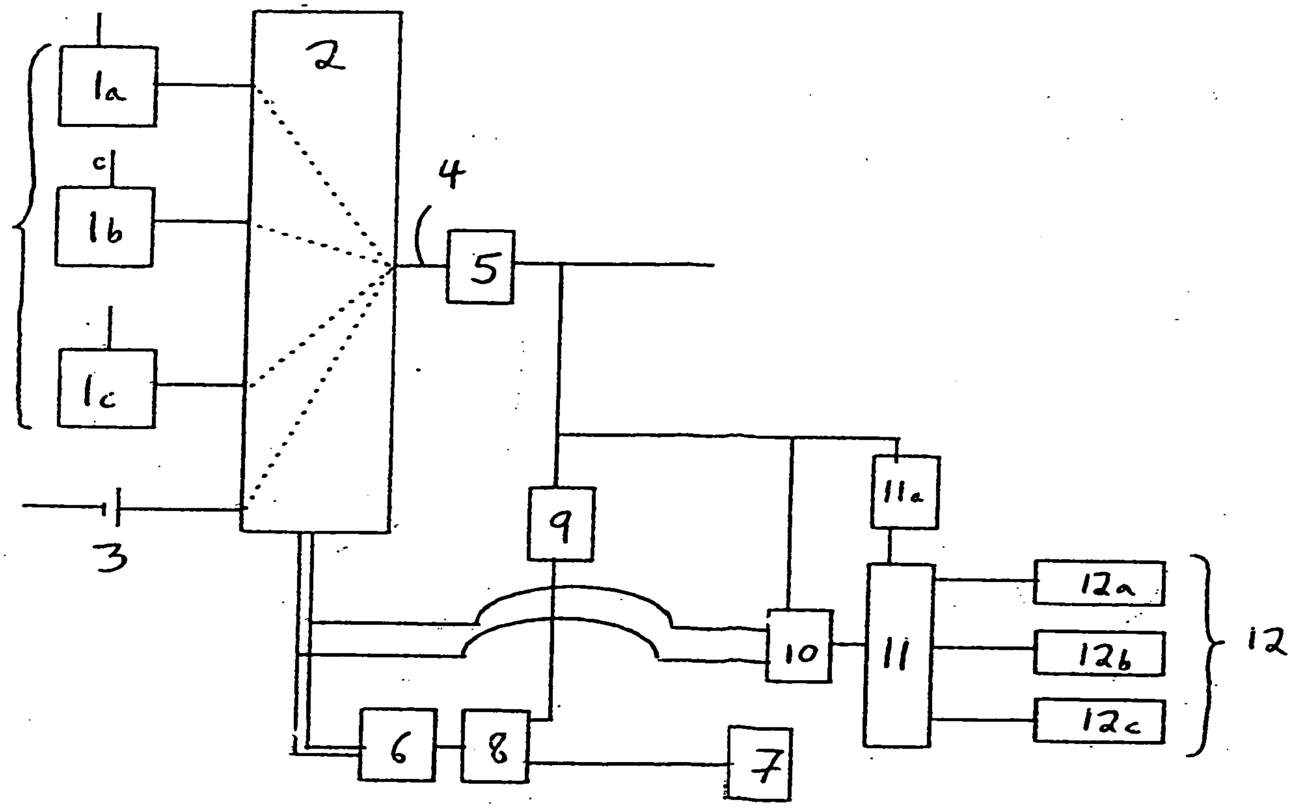


Figure 2

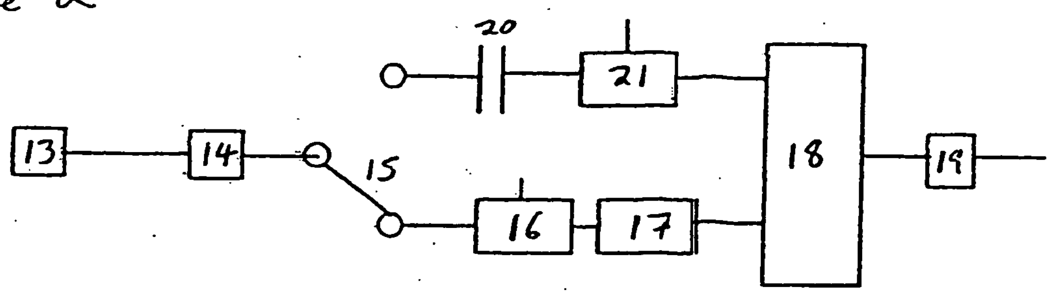


Figure 3a

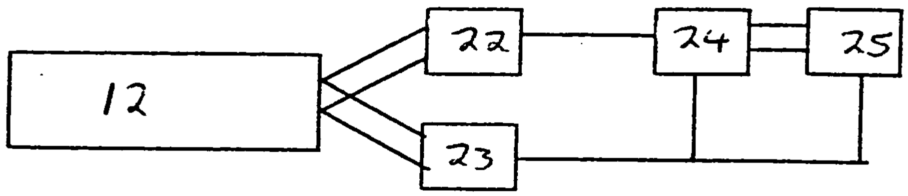


Figure 3b

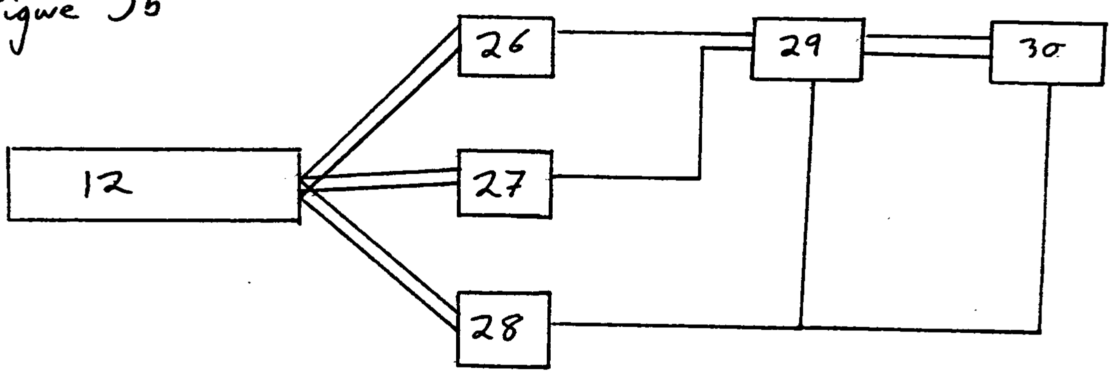
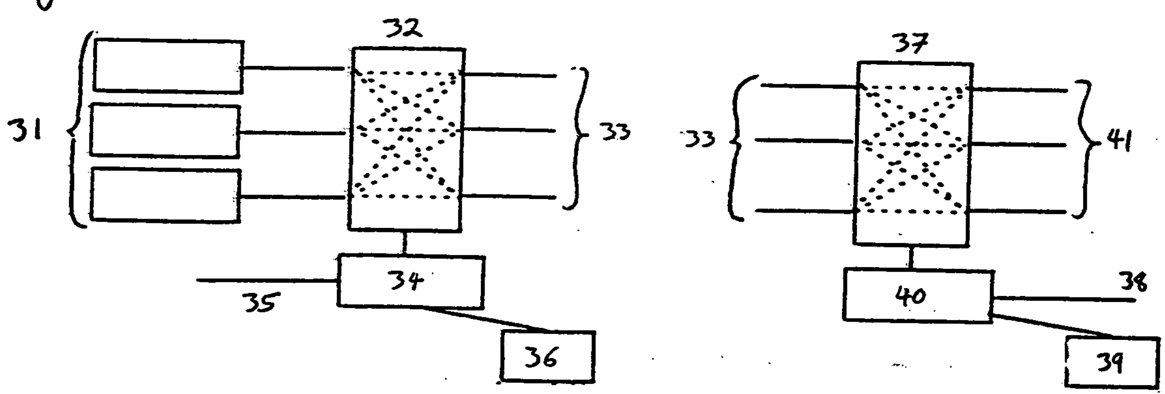


Figure 4



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Marks & Clerk

19 July 00